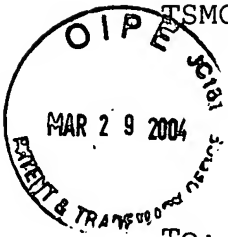


TSMC-03-305



March 19, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/764,913 01/26/04 |
Bor-Wen Chan et al.
A NOVEL METHOD OF TRIMMING
TECHNOLOGY
| _____ |

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 3/25/04

U.S. Patent 6,500,755 to Dakshina-Murthy et al., "Resist Trim Process to Define Small Openings in Dielectric Layers," discloses a photoresist patterned and trimmed on an optical cap layer on a dielectric layer.

U.S. Patent 6,482,726 to Aminpur et al., "Control Trimming of Hard Mask for Sub-100 Nanometer Transistor Gate," discloses a photoresist layer patterned and trimmed above a second hard mask layer.

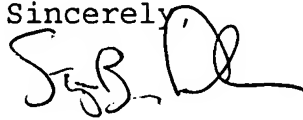
U.S. Patent 6,548,423 to Plat et al., "Multilayer Anti-Reflective Coating Process for Integrated Circuit Fabrication," describes a multilayer anti-reflective coating (ARC) process in which a photoresist layer is patterned and trimmed above a second ARC which is silicon nitride or SiON.

U.S. Patent 6,492,068 to Suzuki, "Etching Method for Production of Semiconductor Devices," describes an etching method in which a photoresist layer is patterned over a bottom ARC (BARC).

U.S. Patent 6,541,360 to Plat et al., "Bi-Layer Trim Etch Process to Form Integrated Circuit Gate Structures," discloses a bilayer trim etch process where a photoresist layer is patterned above an organic layer.

U.S. Patent Application Publication US 2002/0164543 A1 to Lin et al., "Bi-Layer Photolithographic Process," describes a bilayer photolithography process in which an imaging layer is patterned over an underlayer and the pattern is transferred through the underlayer with an O₂/HBr plasma process.

Sincerely,

A handwritten signature in black ink, appearing to read "S.B. Ackerman", with a stylized flourish at the end.

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

Doc No: MUMBAI (Cp 01194)

45466000 Number

TSMC-03-305

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Bor-Wen Chan et al.

Filing Date

01/26/04

Group 27 Unit

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

MAR 29 2004

(Use a verbal shoulds if necessary)

U. S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion, Pages, Etc.)

	U.S. Patent Application Publication US 2002/0164543 A1
	Lin et al., Publication Date 11/7/02, "Bi-layer
	Photolithographic Process", US-Class 430/313,
	filed 7/2/01.

OLIVER

DATE COMPLETED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.